ENGINEERING SPECIFICATION	ES	030467-0	3995
TITLE 1610-3 FUNCTIONAL SPECIFICATION	SHEET 1 OF		

PRODUCT 1610-3

1610-3 FUNCTIONAL SPECIFICATION

ORIGINATOR						APPROVAL			
EC NO	3995								
DATE									

S117 (3/80)

1. SCOPE

This specification defines the design requirements for the Shugart 1610-3 Rigid Disk Controller.

2. APPLICABLE DOCUMENTS

All relevant Engineering Specifications.

Small Computer Systems Interface (ANSI X3T9.2) Specification
ES600 Disk Drive Engineering Specification.
ES700 Disk Drive Engineering Specification.

3. GENERAL DESCRIPTION

3.1 General Description.

The 1610-3 Controller is a microprocessor based rigid disk controller with three custom LSI chips (NMOS). The controller is capable of controlling two Winchester disk drives, ST506 interface compatible. The dimensions of the controller are in the "foot print" of the drives. The custom LSI circuitry is implemented in the Buffer controller chip, Disk controller chip, and Encode/Decode chip. The 1610-3 Controller is designed as a peripheral controller to be used with the low end of the SCSI industry standard interface as defined by the SCSI specification no. (ANSI X3T9.2).

3.2 Features.

* Support subset of SCSI commands on Host Adapter systems without Arbitration.
* Support two different disk drives of the same capacities.
* Up to 1-Mbytes/second maximum bus data transfer rate.
* 5-Mbits/second (ST506) Drive transfer rate.
* 1-KByte Dual Port data buffer.
* Asynchronous REQ/ACK Handshake for bus data transfer.
* Single Ended drivers/receivers.

* Removable bus terminations.
* Implied Seek for data transfer operations.
* 21-Bit logical block addressing.
* Automatic Cylinder/Head switching.
* Programmable sector interleaving.
* Jumper selectable block sizes (256, 512 bytes).
* Multiple block transfer.
* Automatic Read retries.
* Track level defect handling.
* 32-bit ECC polynomial for data field. Allows 11-bit burst error detection and 8-bit burst error correction.
* 16-bit CRC for ID field verification.
* Jumper selectable PULSE-MODE Selection.
* Power On Diagnostic.
* 20,000 hours MTBF

4. DISK DRIVE INTERFACE.

The drive interface is ST506 compatible. The control signals to and from the disk drives are transmitted via a daisy-chain cable at connector J2. Data and clock signals are transmitted differentially between the controller and the drives through the connectors J3 J4, and J5. Figure 4.1 shows the cable configuration between the controller and drives.

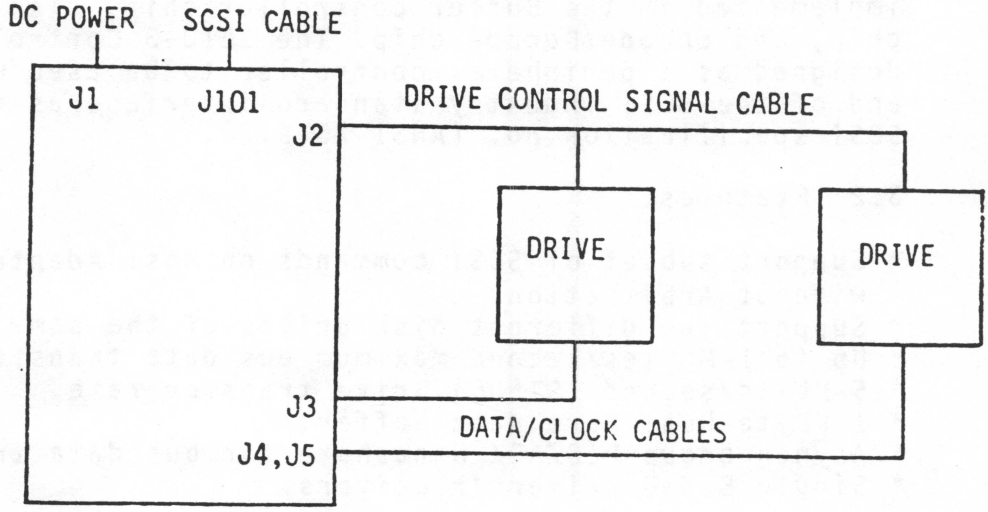


Figure 4.1 1610-3 Drive Cable Configuration.

4.1 Drive Control Signals.

J2 is a 34 pin, control signal, card edge connector. Maximum length should not exceed 20 feet (6 meters). Open collector

drivers are used for all transmitted signals. All assigned control signals are terminated with 220 ohms to +5 volts and 330 ohms to ground at the receiving end of the cable. These termination resistor to be provided by a removable resistor pack. The pin assignment of the J2 connector is shown in Table 4.1.

Table 4.1. J2 Control Signal Cable Pin Assignments

SIGNAL	PIN	DESCRIPTION
-RWC	2	-REDUCE WRITE CURRENT
-HS2	4	-HEAD SELECT BIT 2
-WG	6	-WRITE GATE
-SKC	8	-SEEK COMPLETE
-TK0	10	-TRACK ZERO
-FLT	12	-WRITE FAULT
-HS0	14	-HEAD SELECT BIT 0
	16	SPARE
-HS1	18	-HEAD SELECT BIT 1
-INDX	20	-INDEX
-RDY	22	-DRIVE READY
-STP	24	-STEP
-DS1	26	-DRIVE SELECT 1
-DS2	28	-DRIVE SELECT 2
-DS3	30	-DRIVE SELECT 3
-DS4	32	-DRIVE SELECT 4
-DIR	34	-DIRECTION IN

Note: All odd pins are connected to ground.

4.2 Data and Clock Signals.

J3 and J4 are 20 pin data/clock header pin connectors. J5 is the image of J4 in the form of edge connector. Maximum cable length should not exceed 20 feet (6 meters). Each connector serves one drive. Table 4.2 describes the pin signals of J3 ,J4 and J5.

All assigned data/clock lines are terminated with 100 ohms resistors from each side of the differential line to ground at the receiving end only.

Table 4.2. Data/Clock Signal Cable Pin Assignments.

SIGNAL	PIN	DESCRIPTION
-SEL	1	-DRIVE SELECTED
	2	GROUND
	3	SPARE
	4	GROUND
	5	SPARE
	6	GROUND
	7	SPARE
	8	GROUND
	9	SPARE
	10	SPARE
	11	GROUND
	12	GROUND
+WD	13	+ MFM WRITE DATA
-WD	14	- MFM WRITE DATA
	15	GROUND
	16	GROUND
+RD	17	+ MFM READ DATA
-RD	18	- MFM READ DATA
	19	GROUND
	20	GROUND

4.3 Cable Termination.

The last physical drive at the end of the J2 cable must be terminated.

5. HOST BUS.

The 1610-3 controller communicates with host systems through an interface bus derived from the Small Computer Systems Interface (SCSI). The controller is connected to the host bus via the 50 pin connector at J101. This cable length should not exceed 20 feet (6 meters) from the first to the last device on the bus.

5.1 Interface Signals.

Refer to SCSI Specification (ANSI X3T9.2) for detail description of bus signals.

Table 5.1 shows the pin description of the J101 connector.

Table 5.1. SCSI/SASI Bus Cable Pin Description.

SIGNAL	PIN	DESCRIPTION
-DB0	2	-DATA BUS BIT 0
-DB1	4	-DATA BUS BIT 1
-DB2	6	-DATA BUS BIT 2
-DB3	8	-DATA BUS BIT 3
-DB4	10	-DATA BUS BIT 4
-DB5	12	-DATA BUS BIT 5
-DB6	14	-DATA BUS BIT 6
-DB7	16	-DATA BUS BIT 7
-DP	18	-PARITY, (NOT USED,TERMINATED)
	20	GROUND
	22	GROUND
	24	GROUND
	26	OPEN
	28	GROUND
	30	GROUND
-ATN	32	-ATTENTION N/A
-GND	34	-GROUND
-BSY	36	-BUSY
-ACK	38	-ACKNOWLEDGE Host
-RST	40	-RESET Host
-MSG	42	-MESSAGE
-SEL	44	-SELECT Host
-C/D	46	-CONTROL/DATA
-REQ	48	-REQUEST
-I/O	50	-INPUT/OUTPUT

Note: All odd pins except pin 25 (open) are connected to ground.

5.2 Interface Protocol.

For detailed information regarding the Host Interface Protocol, refer to the SCSI Specification (ANSI X3T9.2)

5.3 Cable Termination.

All assigned signal lines are terminated with 220/330 ohm resistor packs at the controller side. These resistor packs are mounted on sockets to allow for removal if controller is used in the middle of the bus cable.

5.4 Bus Device ID.

The controller is allowed to assume any uniquely assigned SCSI bus device address. This device address (from 0 to 7) can be selected through the jumpers CU4, CU2, CU1. Refer to diagram 6.1 for the location of these jumpers.

6. CIRCUIT BOARD.

The 1610-3 controller consists of a single 2-layer printed circuit board. Figure 6.1 shows the locations of the various cable connectors, removable terminators and option jumpers.

6.1 Option Jumpers.

6.1.1 CU4, CU2, CU1: This group of jumpers are used to set device address of the controller on the SCSI bus.

6.1.2 Jumper W: This jumper is used to select the size of the sectors.

J-W	Bytes/Sec	Sectors/Trk
Out	256	32
In	512	17

6.1.3 Jumpers X and Y: These jumpers are not used.

6.1.4 Jumper Z: This jumper is used in conjunction with the Selection mode jumpers SX, SN and PS. This jumper should be installed if the PULSE MODE is selected. See sections 6.1.7 and 6.1.8.

6.1.5 Jumper H2-H1: These positions if jumpered select

the Hardware Reset mode. When a SCSI host device issues a RESET on the bus, the microprocessor of the controller will be reset. This has the same effect as a power-on reset.

6.1.6 Jumper H2-S: These positions if jumpered select the Software Reset mode. The RESET signal from the host device is latched by the controller. The microprocessor, under program control, would perform a controller reset on the SCSI bus.

6.1.7 Jumper SX-NS: These positions if jumpered select the normal mode of SCSI bus device selection. During the selection phase, the host must continue to assert the SELECT signal until the controller responds with the BUSY signal. If this mode is selected, jumper Z must not be installed.

6.1.8 Jumper SX-PS: This jumper position allows the host adapter to select the controller by pulsing the SELECT line (PULSE MODE). The SELECT signal is latched by the controller allowing the microprocessor to detect that the host initiated selection. This enables the controller to respond to a host that issues short selection pulses. Jumper Z must be installed if this mode is selected.

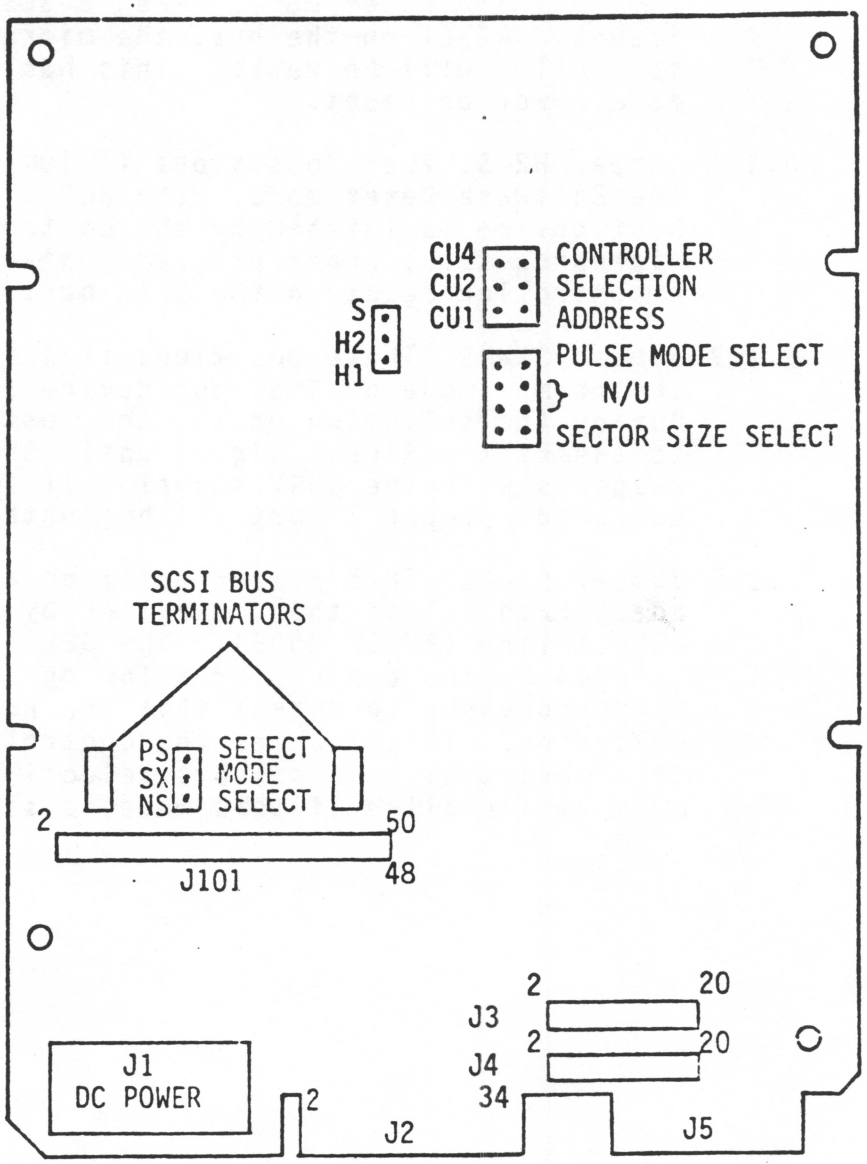


Figure 6.1: 1610-3 Circuit Board Connectors and Option jumpers Locations.

6.2 Physical Specifications.

Width:	5.60 in.	(14.23 cm)
length:	7.75 in.	(19.68 cm)
Height:	0.75 in.	(1.90 cm)
Weight:	8.0 oz.	(0.23 kg)

7. DATA FORMAT.

7.1 Cylinder and Head limits.

Maximum number of cylinders supported is 2048.
Maximum number of heads supported is 8.

7.2 Track Format.

The norminal track capacity is 10,416 bytes; the minimum track capacity is 10,270 bytes (based on a 1.4 percent speed variation).

Figure 7.2 shows the 1610-3 track format. Note that the size of Gap 4 is dependent on the sector size chosen.

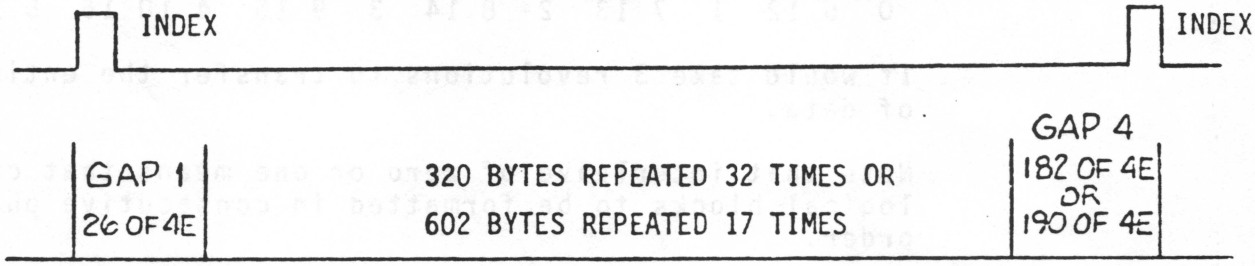


Figure 7.2: Track Format.

7.3 Sector Format.

Figure 7.3.1 shows the sector format. Figure 7.3.2 shows the format of the ID field.

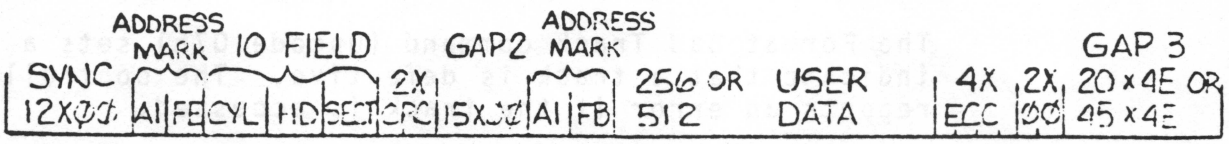


Figure 7.3.1: Sector Format.

C Y L	*X! CYL !Y! HD	SECTOR
	0 0	- Good Track.
	0 1	- Alternate Track.
	1 0	- Bad Track.
	1 1	- Track Alternated.

Figure 7.3.2: ID Field Format.

7.4 Sector Interleave.

Sector interleaving is to tailor host system data transfer speed to disk rotational speed. It allows the host to map contiguous logical blocks on the drive on a non-adjacent physical order. The host system should try different interleave codes to adjust to the maximum data transfer rate.

Example: Interleave code: 3
Maximum sector number: 16

Physical sector:
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17

Logical sector:
0 6 12 1 7 13 2 8 14 3 9 15 4 10 16 5 11 17

It would take 3 revolutions to transfer the entire track of data.

Note that interleave of zero or one means that consecutive logical blocks to be formatted in consecutive physical order.

Interleave code must be less than the number of sectors per track.

7.5 Defect handling.

The 1610-3 controller supports track level defect handling.

The Format Bad Track command (Opcode 07h) sets a flag to indicate that a track is defective. The controller reports an error if the track is accessed.

The controller allows the host to assign a track as an alternate to a track with defect(s). This is done through the Alternate Track command (Opcode 0Eh). Subsequent access to the defective track will cause the controller to access data from the alternate track automatically. Any direct access to the alternate track causes the controller to report an error.

7.6 Write Precompensation and Reduce Write Current.

The host can specify the cylinder number to start performing write precompansation and reduce write current through the Set Drive Parameter Command (Opcode 0Ch).

The controller automatically enables the write precomp circuitry and selects reduce write current mode on the drive at the specified cylinders. If the host does not specify these locations, the defaults at cylinder 128 for the reduce write current and cylinder 64 for the write precompensation.

8. CONTROLLER COMMAND DESCRIPTION

8.1 Command Block.

An Input/Output request to the 1610-3 is performed by passing a command descriptor block (CDB) to the controller. The CDB consists of six bytes sent by the host during the Command phase. The first byte of the CDB is the command group and operation code. The second to the fourth bytes specify such information as the logical unit number (LUN), and block starting address. The fifth byte specifies the number of blocks to transfer. The sixth byte is the Control Byte.

Refer to the SCSI specification (ANSI X3T9.2) for a detailed description of the structure of the command descriptor block.

8.1.1 Logical Unit Number.

The 1610-3 controller supports a maximum of two logical units. Therefore, the LUN field in the command can take on the value of 0 or 1 only.

6.1.2 Control Byte Format.

The 1610-3 controller expects a special format for the control byte. The control byte is the last byte of all commands.

Bit 7: Disable Retry.

If this bit is set, the controller will not attempt to retry the command.

If this bit is reset, upon encountering any error the controller will retry the command.

NOTE: No retry will be performed on the Check Track Format command.

Bit 6: If this bit is set, the controller will not retry a read of a sector that contains data ECC error before attempting correction. The error status (correctable or uncorrectable) is always reported.

If this bit is reset, the controller will reread the sector before attempting to perform ECC data correction. If the error burst is correctable the error will not be reported.

Bit 5: This bit is used in format operation only. If this bit is set, the controller will write the sectors with the data from the sector buffer. User may select the data pattern by first issuing a Write Sector Buffer command (OEh).

Bit 4: This bit is set to indicate that the disk drive has servo information prior to index on each track. During formatting, the controller leaves a gap of 300 microseconds in front of the Index and 40 microseconds following the leading edge of the Index pulse.

Bit 3-0: These four bits are used in combination to select the step rate for the drive. The following step rates are selectable.

BITS 3 2 1 0	DESCRIPTION
0 0 0 0	3 msec step (default, non buffered)
0 0 0 1	Reserved
0 0 1 0	Reserved
0 0 1 1	Reserved
0 1 0 0	200 usec buffered step
0 1 0 1	70 usec buffered step
0 1 1 0	40 usec buffered step
0 1 1 1	40 usec buffered step
1 0 0 0	40 usec buffered step
1 0 0 1	Reserved
1 0 1 0	Reserved
1 0 1 1	Reserved
1 1 0 0	Reserved
1 1 0 1	Reserved
1 1 1 0	Reserved
1 1 1 1	Reserved

Selecting a "Reserved" step rate causes the controller to use the 3 msec step rate.

8.2 Group 0 Commands.

Tables 8.2 shows the different commands under Group 0.

TABLE 8.2: List of Group 0 Commands.

OPCODE	COMMAND
(00)	TEST UNIT READY
(01)	REZERO UNIT
(03)	REQUEST SENSE
(04)	FORMAT UNIT
(05)	CHECK TRACK FORMAT
(06)	FORMAT TRACK
(07)	FORMAT BAD TRACK
(08)	READ
(09)	READ VERIFY
(0A)	WRITE
(0B)	SEEK
(0C)	SET DRIVE PARAMETERS
(0D)	READ ECC BURST ERROR LENGTH
(0E)	ASSIGN ALTERNATE TRACK
(0F)	WRITE SECTOR BUFFER
(10)	READ SECTOR BUFFER

8.2.1 Test Unit Ready Command (00)

TABLE 8.2.1.: TEST UNIT READY COMMAND

	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Byte-0	0	0	0	0	0	0	0	0
Byte-1	----- LUN -----			0	0	0	0	0
Byte-2	(00)							
Byte-3	(00)							
Byte-4	(00)							
Byte-5	(00)							

This command selects and verifies that the LUN specified is powered on and ready. The command returns the zero status if the addressed unit is powered on and ready.

8.2.2 Rezero Unit Command (01)

TABLE 8.2.2.: REZERO UNIT COMMAND

	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Byte-0	0	0	0	0	0	0	0	1
Byte-1	-----	LUN	-----	0	0	0	0	0
Byte-2				(00)				
Byte-3				(00)				
Byte-4				(00)				
Byte-5	(*)	0	0	0	0	0	0	0

(*) See description of Control Byte in section 8.1.

Rezero Unit command recalibrates the unit to track zero (00).

8 2.3 Request Sense Command (03)

TABLE 8.2.3.1.: REQUEST SENSE COMMAND

	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Byte-0	0	0	0	0	0	0	1	1
Byte-1	-----	LUN	-----	0	0	0	0	0
Byte-2				(00)				
Byte-3				(00)				
Byte-4				(00)				
Byte-5				(00)				

The REQUEST SENSE command returns four sense bytes. The sense data will be valid for the Check Condition status just presented to the host. Sense data is preserved by the controller for any check condition status, except immediately after a reset.

A REQUEST SENSE command issued with no Check Condition status logged in will return a zero value in Sense Byte 00.

Check Condition status is never returned for this command.

Following an error indication of the status byte with Check Condition, the host may send a REQUEST SENSE command to obtain more detailed information. The format of the sense bytes returned by the controller is shown in Table 8.2.3.2. For a detailed description of the ADDRESS VALID, CLASS and ERROR CODE, see section 8.5.

TABLE 8.2.3.2.: SENSE BYTES FORMAT

	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Byte-0	AD-VALID	---CLASS (0-3)---			-----ERROR CODE----------			
Byte-1	--------	LUN	-----		----LOGICAL BLOCK ADDR (MSB)----			
Byte-2	----------LOGICAL BLOCK ADDR----------							
Byte-3	----------LOGICAL BLOCK ADDR (LSB)----------							

If Check Condition status is returned after any format command or the CHECK TRACK FORMAT command, the sense data contains the logical block address of the track where the error occurred. If no error occurred and the host issues a REQUEST SENSE command, then the logical block address of the next track is returned in the sense data.

8.2.4 Format Unit Command (04)

TABLE 8.2.4.: FORMAT UNIT COMMAND

	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Byte-0	0	0	0	0	0	1	0	0
Byte-1	----- LUN -----			0	0	0	0	0
Byte-2	(00)							
Byte-3	(00)							
Byte-4	----------INTERLEAVE CODE----------							
Byte-5	(*)	0	(*)	(*)	(*)	(*)	(*)	(*)

(*) See description of the Control Byte in Section 8.1.

The FORMAT UNIT command formats the entire media and ensures that all data blocks can be accessed. Before issuing a FORMAT UNIT command, the host should send the SET DRIVE PARAMETER command to specify the drive characteristics. If the drive parameters are not received, the controller attempts to format the drive with default parameters. Refer to the SET DRIVE PARAMETER command description.

8.2.5 Check Track Format Command (05)

TABLE 8.2.5.: CHECK TRACK FORMAT COMMAND

	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Byte-0	0	0	0	0	0	1	0	1
Byte-1	----- LUN -----			------LOGICAL BLOCK ADDR (MSB)---				
Byte-2	----------LOGICAL BLOCK ADDRESS----------							
Byte-3	----------LOGICAL BLOCK ADDRESS (LSB)--------							
Byte-4	----------INTERLEAVE CODE----------							
Byte-5	(*)	0	0	0	(*)	(*)	(*)	(*)

(*) See description of the Control Byte in Section 8.1.

This command checks the format of the entire track for correctness of all sector ID fields and interleave computation for the track specified by the logical block address. The command does not read the data fields and does not transfer data to the host. The track to be checked is specified by the logical block address of any sector within the track.

8.2.6 Format Track Command (05)

TABLE 8.2.6.: FORMAT TRACK COMMAND

	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Byte-0	0	0	0	0	0	1	1	0
Byte-1	----- LUN -----				----LOGICAL BLOCK ADDR (MSB)---			
Byte-2	----------LOGICAL BLOCK ADDRESS----------							
Byte-3	----------LOGICAL BLOCK ADDRESS (LSB)----------							
Byte-4	----------INTERLEAVE CODE----------							
Byte-5	(*)	0	(*)	(*)	(*)	(*)	(*)	(*)

(*) See description of the Control Byte in Section 8.1.

The FORMAT TRACK command formats all sectors in the track specified by the logical block address of any sector within the track. This operation is similar to the FORMAT UNIT command but limited to one track. User is to ensure that the interleave value set in the CDB is identical to the value previously set for other tracks of the unit.

8.2.7 Format Bad Track (07)

TABLE 8.2.7.: FORMAT BAD TRACK COMMAND

	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Byte-0	0	0	0	0	0	1	1	1
Byte-1	----- LUN -----				----LOGCIAL BLOCK ADDR (MSB)---			
Byte-2	----------LOGICAL BLOCK ADDRESS----------							
Byte-3	----------LOGICAL BLOCK ADDRESS (LSB)----------							
Byte-4	----------INTERLEAVE CODE----------							
Byte-5	(*)	0	0	(*)	(*)	(*)	(*)	(*)

(*) See description of the Control Byte in Section 8.1.

This command formats all sectors of the track specified by the logical block address of any sector within the track as bad sectors.

8.2.8 Read Command (08)

TABLE 8.2.8.: READ COMMAND

	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Byte-0	0	0	0	0	1	0	0	0
Byte-1	----- LUN -----			---LOGICAL BLOCK ADDR (MSB)---				
Byte-2	----------LOGICAL BLOCK ADDRESS----------							
Byte-3	----------LOGICAL BLOCK ADDRESS (LSB)----------							
Byte-4	----------TRANSFER LENGTH----------							
Byte-5	(*)	(*)	0	0	(*)	(*)	(*)	(*)

(*) See description of Control Byte in section 8.1.

The READ command transfers the specified number of blocks to the host beginning at the designated logical starting block address. This command is limited to 21 bits of addressing and 256 blocks of transfer. A value of zero in byte 04 means 256 blocks transfer.

If an unrecoverable error occurs during a multiple sector transfer, the controller terminates the transfer at the sector where the error is encountered.

The controller also terminates a multiple sector transfer if a correctable data error occurs and the NO-RETRY bit (bit-7) of the Control Byte is set. An error status sent to the host.

No data is sent to the host if any error occurred.

8.2.9 Read Verify Command (09)

TABLE 8.2.9.: READ VERIFY COMMAND

	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Byte-0	0	0	0	0	1	0	0	1
Byte-1	----- LUN -----			---LOGICAL BLOCK ADDR (MSB)---				
Byte-2	----------LOGICAL BLOCK ADDRESS----------							
Byte-3	----------LOGICAL BLOCK ADDRESS (LSB)----------							
Byte-4	----------TRANSFER LENGTH----------							
Byte-5	(*)	(*)	0	0	(*)	(*)	(*)	(*)

(*) See description of Control Byte in section 8.1.

This command functions the same as the Read Command, except that no data is sent to the host. This command may be used to verify the data following a write or format operation.

8.2.10 Write Command (0A)

Table 8.2.10.: WRITE COMMAND.

	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Byte-0	0	0	0	0	1	0	1	0
Byte-1	----- LUN -----			---LOGICAL BLOCK ADDR (MSB)---				
Byte-2	----------LOGICAL BLOCK ADDRESS----------							
Byte-3	----------LOGICAL BLOCK ADDRESS (LSB)----------							
Byte-4	----------TRANSFER LENGTH----------							
Byte-5	(*)	0	0	0	(*)	(*)	(*)	(*)

(*) See description of Control Byte in section 8.1.

The WRITE command transfers the specified number of blocks beginning at the designated logical starting block address. This command is limited to 21 bit addressing and 256 blocks of transfer. A value of zero in byte 04 means 256 bytes blocks transfer.

8.2.11 Seek Command (0B)

Table 8.2.11: SEEK COMMAND.

	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Byte-0	0	0	0	0	1	0	1	1
Byte-1	----- LUN -----			---LOGICAL BLOCK ADDR (MSB)---				
Byte-2	----------LOGICAL BLOCK ADDRESS----------							
Byte-3	----------LOGICAL BLOCK ADDRESS (LSB)----------							
Byte-4	(00)							
Byte-5	(*)	0	0	0	(*)	(*)	(*)	(*)

(*) See description of Control Byte in section 8.1.

The SEEK command requests the unit to prepare itself to transfer data from the specified address in minimal time. As READ and WRITE commands are performed with implied seek, it is not mandatory to use this command. The command is limited to 21 bit addressing.

If Buffered Step mode is specified in the Control Byte, the controller will issue the seek step pulses to the disk drive and report command complete to the host before receiving SEEK COMPLETE status from the drive. This allows the user to perform overlap seek operations. If another command is issued by the host for the drive unit that is still seeking, then the controller will wait until the seek is completed before executing the new command.

The TEST UNIT READY command can be used during Buffer Step mode to determine if a seek request is completed. A Check Condition status is returned if the drive is still seeking. The returned sense data is DRIVE STILL SEEKING (Class:0 Code:8).

8.2.12 Set Drive Parameters Command (0C).

TABLE 8.2.12.1: SET DRIVE PARAMETER COMMAND

	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Byte-0	0	0	0	0	1	1	0	0
Byte-1				(00)				
Byte-2				(00)				
Byte-3				(00)				
Byte-4				(00)				
Byte-5				(00)				

The host specifies the disk parameters of the drives connected to the controlller by sending the SET DRIVE PARAMETER command. This should be done after power-on or a RESET to the controller. The drive parameters are sent to the controller during the DATA OUT phase of the command execution. The parameters are stored in the controller RAM.

The pararameters and characteristics of both drives connected to the controller are initialized when this command is issued. Therefore, if drives with different parameters are used, this command must be sent to the controller each time when switching between drive.

The format of the drive parameter block is described in Table 8.2.12.2.

Table 8.2.12.2: Drive Parameter Format.

Byte-0:	Maximum number of Cylinders (MSB).
Byte-1:	Maximum number of Cylinders (LSB).
Byte-2:	Maximum number of Heads.
Byte-3:	Reduce Write Current Cylinder (MSB).
Byte-4:	Reduce Write Current Cylinder (LSB).
Byte-5:	Write Precompensation Cylinder (MSB).
Byte-6:	Write Precompensation Cylinder (LSB).
Byte-7:	Maximum ECC data burst length

The maximum number of cylinders and heads supported by the 1610-3 controller is defined in Section 7.1 of this document.

Upon reset or power-up, the controller defaults to the drive parameters as shown in table 8.2.12.3.

Table 8.2.12.3: Default Drive Parameters.

	HEX VALUE	
Byte-0:	00	
Byte-1:	99	Maximum number of Cylinders = 153.
Byte-2:	04	Maximum number of Heads = 4.
Byte-3:	00	
Byte-4:	80	Reduce Writer Current Cylinder = 128.
Byte-5:	00	
Byte-6:	40	Write Precompensation Cylinder = 64.
Byte-7:	08	Maximum ECC data burst length correctable = 8 bits. (Any larger value defaults to 8.)

8.2.13 Read ECC Burst Error Length Command (0D).

TABLE 8.2.13.1: READ ECC BURST ERROR LENGTH COMMAND

	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Byte-0	0	0	0	0	1	1	0	1
Byte-1				(00)				
Byte-2				(00)				
Byte-3				(00)				
Byte-4				(00)				
Byte-5				(00)				

This command transfers one byte of information to the host indicating the ECC burst error length of an error just encountered. This command is only valid immediately following a Correctable Data Error code (18h).

8.2.14 Assign Alternate Track Command (0E)

TABLE 8.2.14.1: ASSIGN ALTERNATE TRACK COMMAND

	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Byte-0	0	0	0	0	0	1	1	1
Byte-1	----- LUN -----				----LOGCIAL BLOCK ADDR (MSB)---			
Byte-2	----------LOGICAL BLOCK ADDRESS----------							
Byte-3	----------LOGICAL BLOCK ADDRESS (LSB)----------							
Byte-4	----------INTERLEAVE CODE----------							
Byte-5	(*)	0	(*)	(*)	(*)	(*)	(*)	(*)

(*) See description of the Control Byte in Section 8.1.

The ASSIGN ALTERNATE TRACK command allocates an alternate track (whose address is specified in a 3 byte field sent in the DATA OUT phase of the command) to the track specified by the logical block address in the CDB. The controller modifies the format of both the alternated and the alternate track by changing the ID fields of all sectors of those tracks.

Table 8.2.14.2 shows the format of the 3 byte field that is sent during the DATA OUT phase to specify the alternate track address

TABLE 8.2.14.2: ALTERNATE TRACK ADDRESS

	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Byte-0	0	0	0	----LOGCIAL BLOCK ADDR (MSB)---				
Byte-1	----------LOGICAL BLOCK ADDRESS----------							
Byte-2	----------LOGICAL BLOCK ADDRESS (LSB)----------							

Attempts to access the logical block(s) of a track that is alternated causes the controller to access the blocks at the alternate track. Attempts to access any sector in the alternate track directly causes a CHECK CONDITION status.

Alternate tracks cannot be allocated as alternated tracks to other alternate tracks. Only one level of assignment is allowed. A track cannot be alternated to itself.

8.2.15 Write Sector Buffer Command (0F).

TABLE 8.2.15: WRITE SECTOR BUFFER COMMAND

	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Byte-0	0	0	0	0	1	1	1	1
Byte-1				(00)				
Byte-2				(00)				
Byte-3				(00)				
Byte-4				(00)				
Byte-5				(00)				

This command allows the user to send to the controller RAM buffer a sector of data.

After issuing this command, subsequent format operation may write disk with the data in the buffer, if bit 5 in the control byte of the format command block is set.

This command may also be used to test the RAM memory by writing a test pattern and reading it back with the Read Sector Buffer command.

8.2.16 Read Sector Buffer Command (10).

TABLE 8.2.16.1: READ SECTOR BUFFER COMMAND

	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Byte-0	0	0	0	1	0	0	0	0
Byte-1				(00)				
Byte-2				(00)				
Byte-3				(00)				
Byte-4				(00)				
Byte-5				(00)				

The controller will not send the data to the host if an uncorrectable data error is detected. Therefore, this command may be used to retrieve the data in the controller's buffer.

This command is also used to test the RAM buffer.

8.3 Group 7 Commands.

Tables 8.3 shows the Group 7 commands supported by the 1610-3 controller.

TABLE 8.3: List of Group 7 Commands.

OPCODE	COMMAND
(E0)	RAM DIAGNOSTIC
(E3)	DRIVE DIAGNOSTIC
(E4)	CONTROLLER DIAGNOSTIC
(E7)	REQUEST LOGOUT

8.3.1 RAM Diagnostic Command (E0).

TABLE 8.3.1.: RAM DIAGNOSTIC COMMAND

	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Byte-0	1	1	1	0	0	0	0	0
Byte-1				(00)				
Byte-2				(00)				
Byte-3				(00)				
Byte-4				(00)				
Byte-5				(00)				

This command performs a data pattern test on the internal controller 1K RAM. The controller automatically performs this function at power-up.

8.3.2 Drive Diagnostic Command (E3).

TABLE 8.3.2.: DRIVE DIAGNOSTIC COMMAND

	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Byte-0	1	1	1	0	0	0	1	1
Byte-1				(00)				
Byte-2				(00)				
Byte-3				(00)				
Byte-4				(00)				
Byte-5				(00)				

This diagnostic command reads sector zero on all tracks sequentially.

8.3.3 Controller Diagnostic Command (E4).

TABLE 8.3.3.: CONTROLLER DIAGNOSTIC COMMAND

	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Byte-0	1	1	1	0	0	1	0	0
Byte-1				(00)				
Byte-2				(00)				
Byte-3				(00)				
Byte-4				(00)				
Byte-5				(00)				

This command causes the controller to perform an internal diagnostic. The controller first verifies the checksum of the EPROM. The ECC circuitry is then tested by shifting in a data pattern and verifying the ECC pattern generated.

8.3.4 Request Logout Command (37).

TABLE 8.3.4.1: REQUEST LOGOUT COMMAND

	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Byte-0	1	1	1	0	0	1	1	1
Byte-1	------LUN------			0	0	0	0	0
Byte-2	(00)							
Byte-3	(00)							
Byte-4	(00)							
Byte-5	(00)							

The controller keeps track of the error statistics for each connected drive. This command causes the controller to return the 8 bytes of error statistics associated with the specific LUN during the DATA IN phase. The format of the error statistics returned is shown in Table 8.3.4.2.

The error log area is cleared after completing this command.

Table 8.3.4.2: Error Logout Data Format.

Byte-0: Non-recoverable Error Count (MSB).
Byte-1: Non-recoverable Error Count (LSB).
Byte-2: Recoverable Errors (MSB).
Byte-3: Recoverable Errors (LSB).
Byte-4: Soft ECC Errors (MSB).
Byte-5: Soft ECC Errors (LSB).
Byte-6: Correctable ECC Errors (MSB).
Byte-7: Correctable ECC Errors (LSB).

- Non-recoverable errors are errors that cannot be overcome after all retries, except unrecoverable ECC errors.

- Recoverable errors are ones that are overcome after one or more retries. This count excludes the recoverable ECC errors.

- Soft ECC errors are ECC errors that are detected on the first read operation which are then read with no errors during retry operations.

- Correctable ECC errors are errors that are correctable using the ECC correction scheme.

8.4 Completion Status Byte.

When the 1610-3 controller completes a command, a byte of status is always sent to the host during the STATUS phase. This is used to indicate to the host if the command is completed successfully.

The format of the status byte is shown in Table 8.4.

Table 8.4.: Status Byte Format.

Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
<-------LUN------->			0	0	0	ERROR	0

- Bit-1: ERROR; This bit is set if an error occured during command execution. The host may perform a REQUEST SENSE command (03) to obtain more detailed information.

8.5 Sense Bytes Format.

The REQUEST SENSE command (03) returns a block of four bytes of sense information to the host. See Section 8.2.3.

The first byte of the sense data contains the following fields:

- Bit-7: ADDRESS VALID; If set, then bytes 01 through 03 of the sense data represent the address at which the error occurred.

- Bit-4 to 6: CLASS; Specifies the error class.

- Bit-0 to 3: ERROR CODE; Specifies the type of error.

8.5.1 Class 0: Drive Error Codes.

HEX VALUE	
(0)	No Sense.
(1)	No Index Signal From Drive Selected.
(2)	No Seek Complete.
(3)	Drive Fault.
(4)	Drive Not Ready.
(5)	Not Used.
(6)	No Track 00.
(7)	Not Used.
(8)	Seek In Progress.
(9 - F)	Not Used.

8.5.2 Class 1: Controller Error Codes.

HEX VALUE	
(0)	ID CRC Error.
(1)	Uncorrectable Data Error.
(2)	ID Address Mark Not Found.
(3)	Not Used.
(4)	Record Not Found.
(5)	Seek Error.
(8)	Correctable Data Check.
(9)	Bad Block Found.
(A)	Format Error.
(B)	Not Used.
(C)	Direct Access to an Alternate track.
(D)	Alternate track already assigned.
(E)	Assigned track of an Alternated track not formatted as an Alternate track.
(F)	The Alternate track is assigned to itself on an Assign Alternate Track command.

8.5.3 Class 2: Command Error Codes.

(0)	Invalid Command.
(1)	Illegal Block Address.
(2)	Illegal Function for Current Drive Type.
(3 - F)	Not Used.

8.5.4 Class 3: Miscellenous Error Codes.

(0)	RAM error, Detected During Diagnostic.
(1)	EPROM Checksum error.
(2)	ECC diagnostic error.
(3 - F)	Not Used.

9.1 Environmental Specifications

	Storage	Transit	Non-Oper.	Operating
Temp.	-40 to 140oF (-40 to 60oC)	-40 to 140oF (-40 to 60oC)	50 to 115oF (10 to 46oC)	50 to 115oF (10 to 46oC)
Temp. Gradient	27oF/hr (15oC/hr)	27oF/hr (15oC/hr)	18oF/hr (10oC/hr)	18oF/hr (10oC/hr)
Relative Humidity	10 - 95% No Condensation.	10 - 95% No Condensation.	10 - 80% No Condensation.	10 - 80% No Condensation.
Humidity Gradient	10%/hr	10%/hr	10%/hr	10%/hr
Altitude	0-40,000ft. (0-12,192 m)	0-40,000ft. (0-12,192 m)	0-40,000ft. (0-12,192 m)	0-10,000ft (0-3,048 m)

The controller normally does not require fans in standard operating environments where airflow is not restricted.

9.2 Power Requirements.

J1 is a four pin connector which supplies DC power to the controller. Table 8.2 shows the pin assignment for this connector.

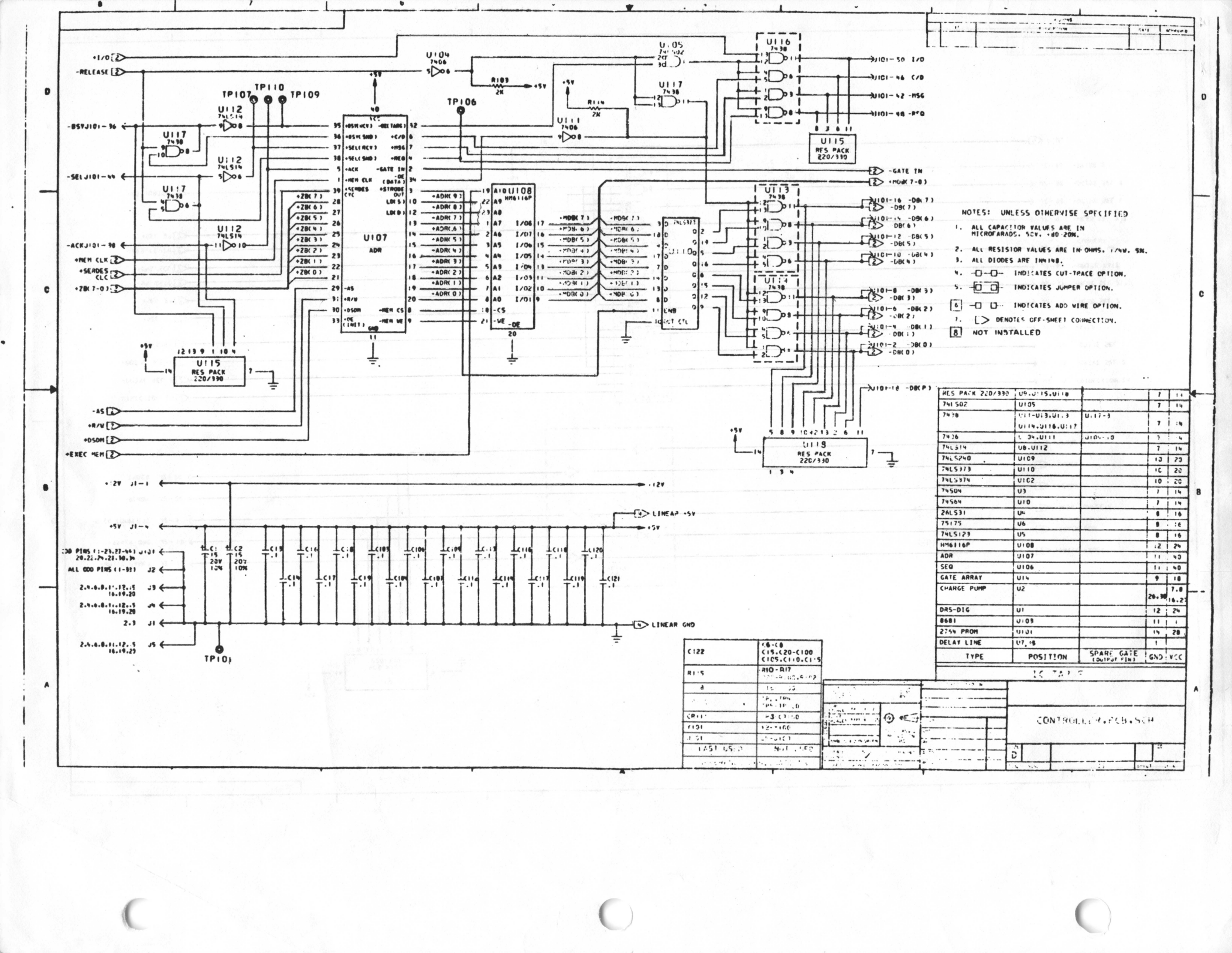
Table 8.2: J1 Connector Power Requirements

Pin	Voltage	Current Nom	Current Max	Ripple
1	+12VDC (+/-5%)	40 ma	50 ma	100 mv
2	+12V RETURN			
3	+ 5V RETURN			

9.3 Compatibility

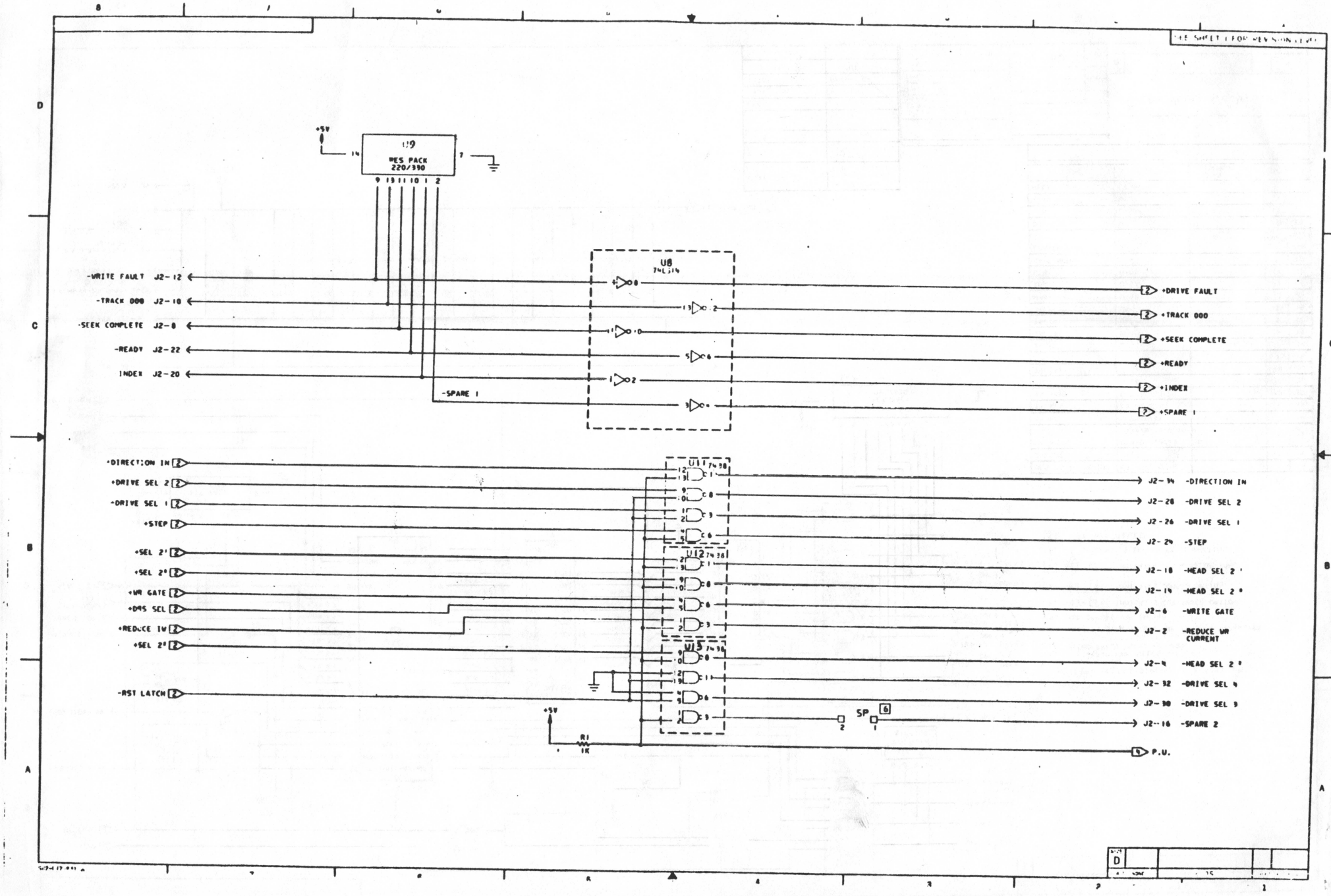
The 1610-3 controller is designed to be compatible with the Xebec S1410A which runs with the standard firmware set (Xebec P/N 104788). Due to hardware limitations and differences, the 1610-3 controller differs from the Xebec S1410A as follows:

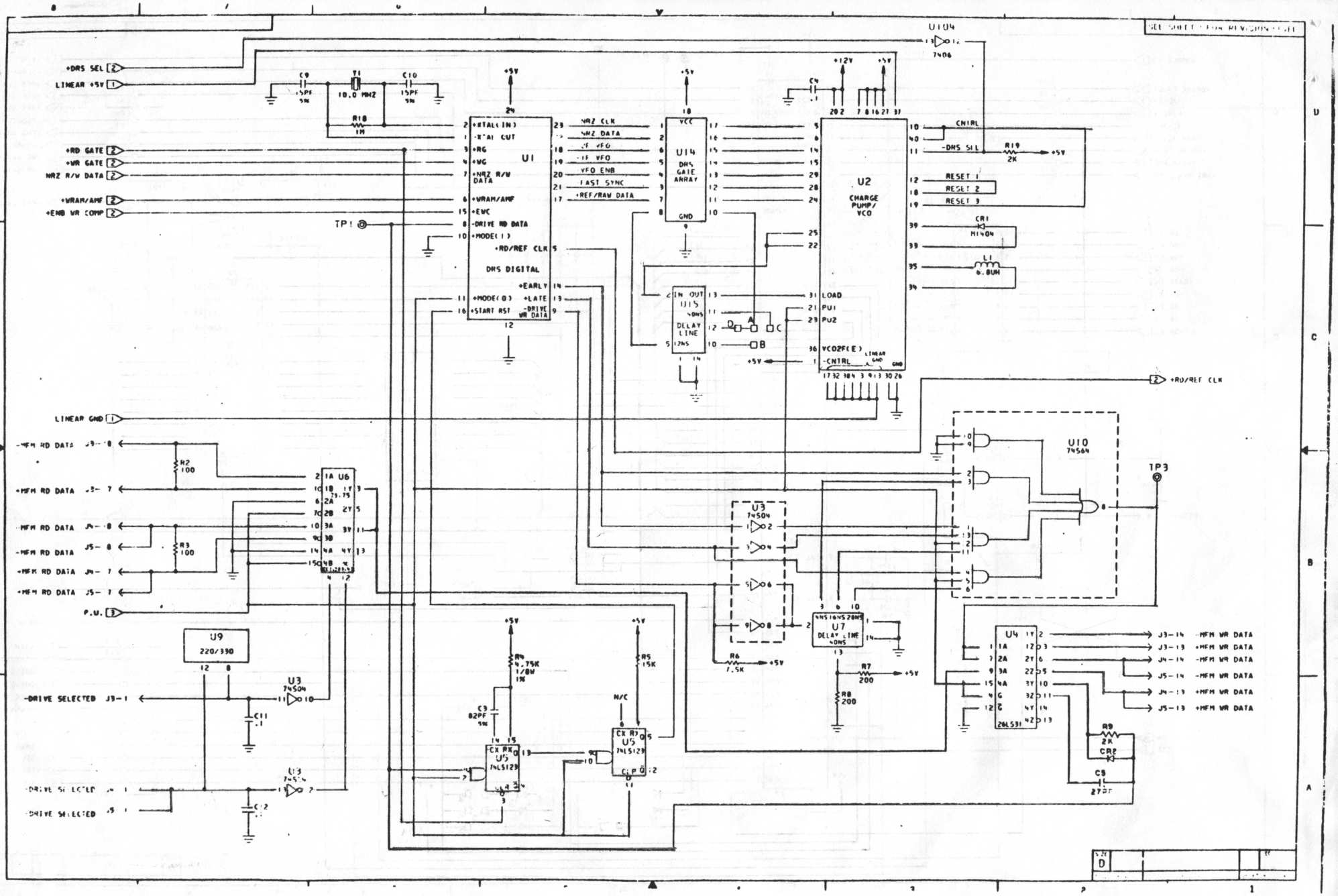
1610-3	S1410A with standard firmware
- Commands not supported: Diagnostic Read Long and Diagnostic Write Long.	N/A
- Number of heads supported: 8 Heads	16 Heads
- Supported step rates: 3 mSec, 200 uSEc, 70 uSec, and 40 uSec.	3 mSec, 200 uSec, 70 uSec, 30 uSec, 15 uSec and 12 uSec.
- Write precompensation values: 0 or +/- 12 nSec.	Determined by bit P (MSB of write precomp. parameters) as follows: P = 0: 0 or +/- 5 nSec P = 1: 5 or +/- 15 nSec.
- Selection phase timing:	
Minimum time for assertion of SEL signal: . 50 uSec: normal mode . 100 nSec: pulse mode (limited to 1 controller per SCSI bus).	100 nSec
BSY responses to SEL: 50 uSec	50 nSec.
- ECC error burst length: 8 bits Max.	11 bits Max. (1000 times higher probability of miscorrection).
- Power requirements: + 5.0 VDC at 1.7 A Max. +12.0 VDC at .05 A Max.	+ 5.0 VDC at 1.3 A Max. +12.0 VDC at .006 A Max.

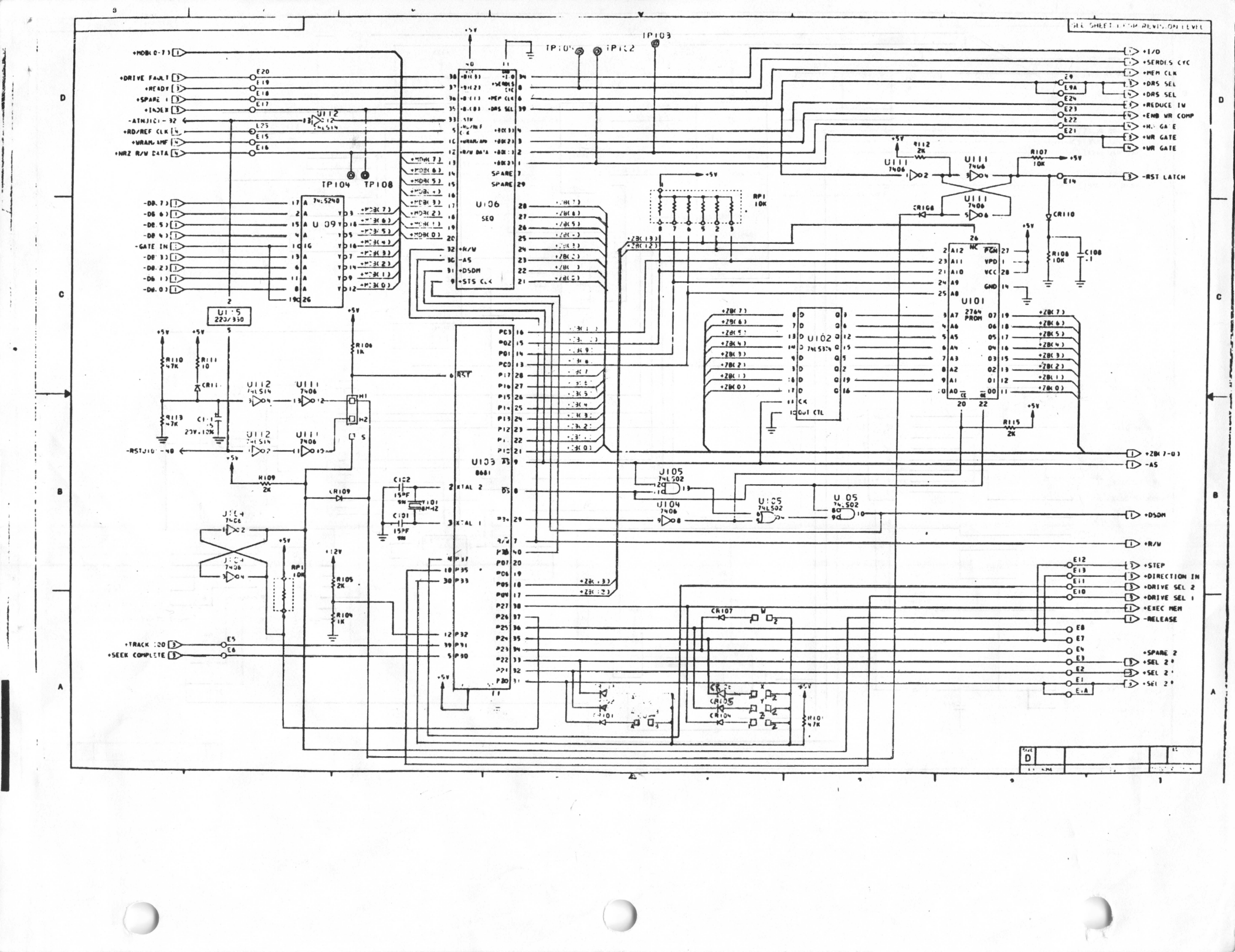


RES PACK 220/330	U8,U115,U119		7	14
74LS02	U105		7	14
7438	U117-U118,U11-3 U119,U116,U117	U117-3	7	14
7406	U104,U111	U104-10	7	14
74LS14	U8,U112		7	14
74LS240	U109		10	20
74LS373	U110		10	20
74LS374	U102		10	20
74S04	U3		7	14
74S64	U10		7	14
26LS31	U4		8	16
75175	U6		8	16
74LS123	U5		8	16
HM6116P	U108		12	24
ADR	U107		11	40
SEQ	U106		11	40
GATE ARRAY	U14		9	18
CHARGE PUMP	U2		20,30	7,8 16,23
DRS-DIG	U1		12	24
8681	U109		11	1
2764 PROM	U101		14	28
DELAY LINE	U7,16		1	
TYPE	POSITION	SPARE GATE (OUTPUT PIN)	GND	VCC

C122	C6-C8 C15,C20-C100 C105,C110,C115
R115	R10-R17
[illegible]	[illegible]
[illegible]	[illegible]
[illegible]	[illegible]
[illegible]	[illegible]
LAST USED	NOT USED


+5V
U9
RES PACK
220/390
14
7
9 13 11 10 1 2
U8
74LS14
-WRITE FAULT J2-12
-TRACK 000 J2-10
-SEEK COMPLETE J2-8
-READY J2-22
INDEX J2-20
-SPARE 1
+DRIVE FAULT
+TRACK 000
+SEEK COMPLETE
+READY
+INDEX
+SPARE 1
+DIRECTION IN
+DRIVE SEL 2
+DRIVE SEL 1
+STEP
+SEL 2'
+SEL 2°
+WR GATE
+DAS SEL
+REDUCE IW
+SEL 2³
-RST LATCH
U11 74S38
U12 74S38
U15 74S38
J2-34 -DIRECTION IN
J2-28 -DRIVE SEL 2
J2-26 -DRIVE SEL 1
J2-29 -STEP
J2-18 -HEAD SEL 2 '
J2-14 -HEAD SEL 2 °
J2-6 -WRITE GATE
J2-2 -REDUCE WR CURRENT
J2-4 -HEAD SEL 2 ³
J2-32 -DRIVE SEL 4
J2-30 -DRIVE SEL 3
J2-16 -SPARE 2
P.U.
SP
R1
1K


U104
7406
+DRS SEL
LINEAR +5V
C9
15PF
5%
Y1
10.0 MHZ
C10
15PF
5%
R18
1M
U1
DRS DIGITAL
+XTAL IN
-XTAL OUT
+RG
+VG
+NRZ R/W DATA
+VRAM/AMP
+EWC
-DRIVE RD DATA
+MODE( )
+RD/REF CLK
+EARLY
+LATE
-DRIVE WR DATA
+MODE(0)
+START RST
+RD GATE
+WR GATE
NRZ R/W DATA
+VRAM/AMP
+EWC WR COMP
TP1
U14
DRS GATE ARRAY
VCC
GND
NRZ CLK
NRZ DATA
+F VFO
-F VFO
VFO ENB
FAST SYNC
+REF/RAW DATA
U2
CHARGE PUMP/ VCO
LOAD
PU1
PU2
VCO2FC(E)
-CNTRL
LINEAR GND
CNTRL
-DRS SEL
R19
2K
RESET 1
RESET 2
RESET 3
CR1
MI404
L1
6.8UH
U15
DELAY LINE
40NS
12NS
+RD/REF CLK
LINEAR GND
-MFM RD DATA J3-8
+MFM RD DATA J3-7
-MFM RD DATA J4-8
-MFM RD DATA J5-8
+MFM RD DATA J4-7
+MFM RD DATA J5-7
P.U.
R2
100
R3
100
U6
75175
U10
74S64
TP3
U3
74S04
U9
220/390
-DRIVE SELECTED J3-1
-DRIVE SELECTED J4-1
-DRIVE SELECTED J5-1
C11
.1
C12
.1
R4
4.75K
1/8W
1%
R5
15K
N/C
C3
82PF
5%
U5
74LS123
R6
7.5K
U7
DELAY LINE
40NS
R7
200
R8
200
U4
26LS31
J3-14 -MFM WR DATA
J3-13 +MFM WR DATA
J4-14 -MFM WR DATA
J5-14 -MFM WR DATA
J4-13 +MFM WR DATA
J5-13 +MFM WR DATA
R9
2K
CR2
C8
270PF
SIZE
D


U106
SEQ
U109
74LS240
U101
2764 PROM
U102
74LS374
U103
8081
U105
74LS02
U104
7406
U112
74LS14
U111
7406
U115
220/330
RP1
10K
TP103
TP104
TP108
+5V
+12V
+MDB(0-7)
+DRIVE FAULT
+READY
+SPARE 1
-ATN/ICI-92
+RD/REF CLK
+WRAP AMP
+NRZ R/W DATA
-DB(7)
-DB(6)
-DB(5)
-DB(4)
-GATE IN
-DB(3)
-DB(2)
-DB(1)
-DB(0)
+ZB(7)
+ZB(6)
+ZB(5)
+ZB(4)
+ZB(3)
+ZB(2)
+ZB(1)
+ZB(0)
+R/W
-AS
+DSDM
+STS CLK
+I/O
+SERDES CYC
+MEM CLK
+DRS SEL
+REDUCE IN
+ENB WR COMP
+WR GATE
-RST LATCH
+STEP
+DIRECTION IN
+DRIVE SEL 2
+DRIVE SEL 1
+EXEC MEM
-RELEASE
+SPARE 2
+SEL 2 0
+SEL 2 1
+SEL 2 2
+TRACK 00
+SEEK COMPLETE
-RST/IC -40
XTAL 1
XTAL 2
RST
Out CTL
15MHZ
15PF
23V,10%